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Effect of High Temperature on the Impact Ionization of N-Channel Fully Depleted SOI MOSFET

K. Ullah, S. Riaz, M.Habib, F. Abbas, S. Naseem, G. Abbas

***Abstract*—** High temperature effects on the impact ionization of the n-channel fully depleted (FD) SOI MOSFET are investigated over a wide range of temperature from 300 to the 600 K by using TCAD. In particular, we have studied the current voltage characteristics (Id-Vd and Id-Vg) , threshold voltage (Vth)and transconductance (gm). By the simulation results, we have analyzed that impact ionization decreases with increasing the temperature and vice versa. Furthermore, we have observed that threshold voltage and transconductance are both inversely proportional to the temperature.

***Keywords*—** Impact Ionization, Fully Depleted, TCAD Transconductance.

I. INTRODUCTION

The dimensions of Silicon on Insulator (SOI) MOSFET have been scaled down by year to year in order to achieve the high performance of the device [1]. SOI thickness (t_{si})is the main parameter because due to scaling the short channel effect reduces [2]. The main advantages of the SOI MOSFET are containing the improved isolation, reduced drain to source capacitance, low operating voltage and faster switching signals [3].Many authors reported the effects of temperature on the SOI devices. Some have developed the temperature dependent model for the fully depleted (FD) SOI MOSFET [4]. A few authors have compared the high temperature effects of fully depleted and partially depleted with bulk CMOS devices [5].

In our work, we have studied the effects of temperature on the impact ionization, threshold voltage (Vth), transconductance (gm). With the rise of temperature impact ionization phenomenon is reducing. The reason is that due to phonon scattering mobility of the carriers reduced due to which the drain current reduces. By the reduction of the drain current, impact ionization phenomenon decreases. By the simulating results from TCAD, it has observed that threshold voltage decreases with increasing the temperature. The reason is that at low temperature the Fermi potential increases so the carriers required high energy to cross that barrier that' s why the threshold voltage increases at lower temperature. Furthermore, we have observed that transconductance decreases if increase the temperature the reason is that drain current decreases with increasing the temperature.

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II. STIMULATED STRUCTURE

Figure 1 shows a cross-sectional view of the n-Channel FD SOI MOSFET. We have used the hydrodynamic model for the carrier transportation and UNIBO2 model which accounts for the impact ionization

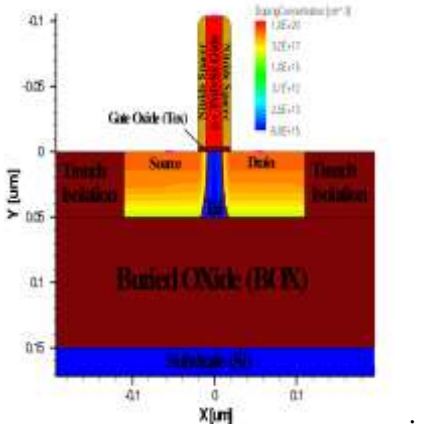

Figure 1. shows a cross-sectional view of the n-channel FD SOI MOSFET

For the designing of the device we use Sentaurus structure editor for the simulation of structure of device. To design a device the important feature to keep in mind are high saturation current and low on resistance.The n-Channel FD SOI-MOSFET with t_{Si}= 50 nm is simulated.Gate oxide thickness (t_{ox}) is 5 nm, buried oxide (BOX) thickness (t_{BOX}) is 100 nm, and doping concentration in the substrate under the BOX (N_{sub}) is $1x10^{15}cm^{-3}$. We take the doping concentration of drain/source is $1\times10^{18}cm^{-3}$ and of gate is $1\times10^{20}cm^{-3}$. The gate length and height is selected to be 20 and 100 nm respectively.

III. Results and Discussions

Figure 2 shows the Id-Vgcurves for the n-channel FD SOI MOSFET at the temperature range of 300 to 600 K at fixed doping concentration of the channel. At lower temperature the value of drain current is greater whether at higher temperature drain current is small. The reason is that at higher temperature the scattering is very large between lattice atom and electron which degrade the mobility. Due to this flow of carriersslowed down and drain current decreases [6]. At lower temperature there is less degradation of mobility therefore the drain current increases as shown in figure.

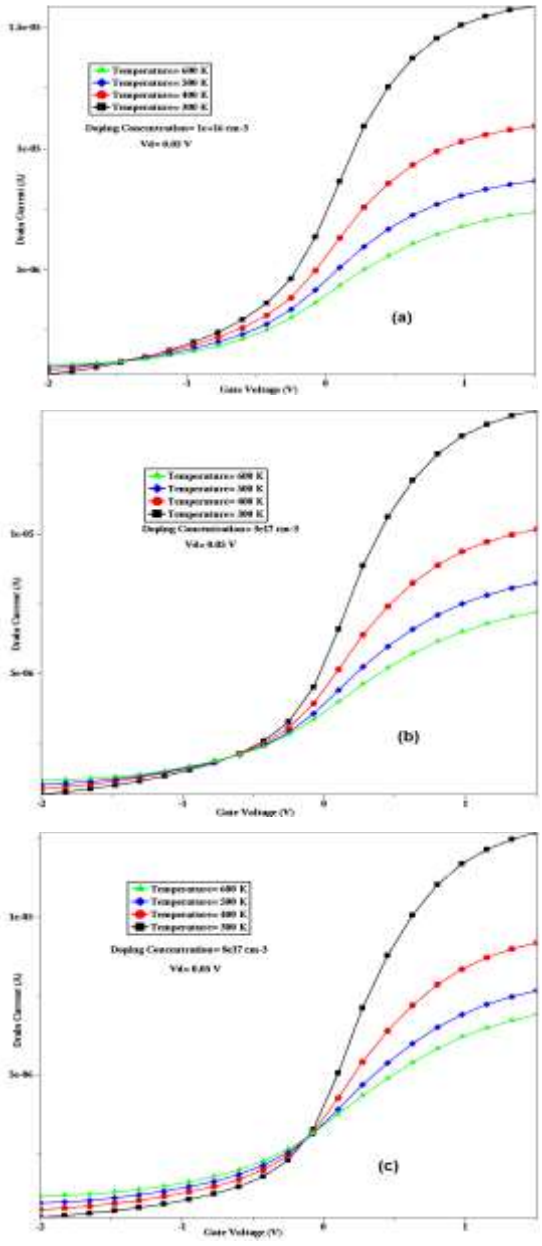

Figure 2. Id-Vg characteristics curvesat 300 K with channel doping concentration (a)$1\times10^{16}cm^{-3}$, (b) $3\times10^{17}cm^{-3}$(c)$8\times10^{17}cm^{-3}$

Figure 3 shows the effect of temperature on Id-Vd curves on fixed doping concentrations. At lower temperature the value of drain current is high whereas at higher temperature current's value is low [7]. For the concentration of 1×1016cm-3, at drain voltage of 5 V when temperature is 300 K, the value of drain current was 0.00475 A whereas at 600 K its value was 0.00310 A. The reason behind this is that there are mainly three scattering mechanism in the SOI MOSFET named as coulomb scattering, phonon scattering and surface roughness scattering. Surface roughness scattering is independent of the temperature whereas coulomb scattering and phonon scattering are temperature dependent [8]. Due to these two temperatures dependent scattering there is large mobility degradation at higher temperature that's why a very low value of drain current is attained at higher temperature.

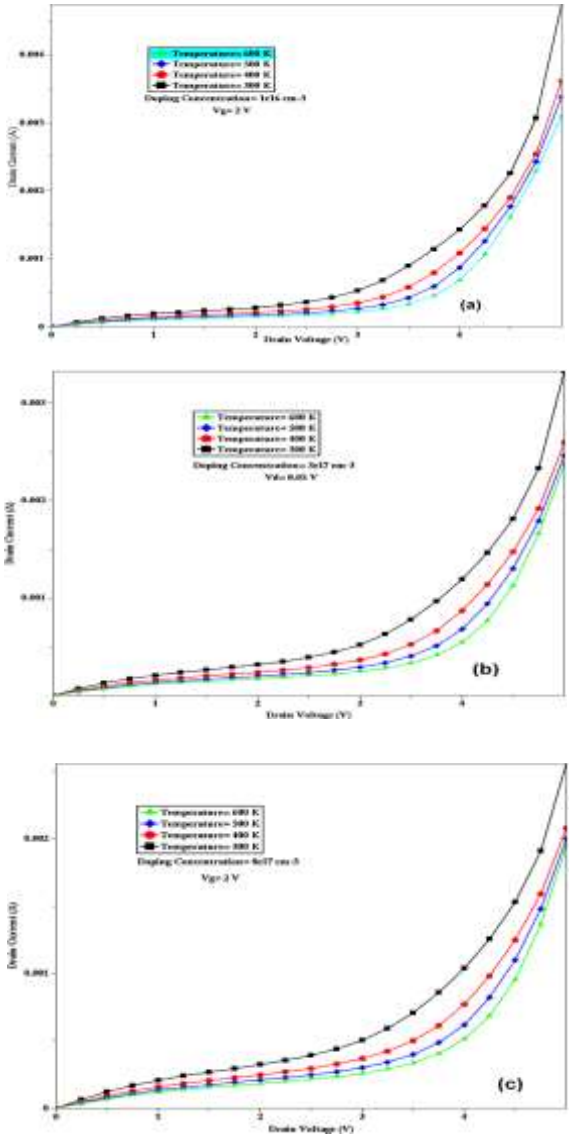

Figure 3. Id-Vg curvesat 300 K with channel doping concentration (a)1×1016cm-3,(b) 3×1017cm-3(c) 8×1017cm-3

Figure 4 shows that threshold voltage decreases with the increase of the temperature. The reason is that at low temperature there is a large Fermi potential that's why the device required more struggle to cross this barrier therefore the

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threshold voltage of the device increases with the decreases of the temperature [9]. When the temperature increases then there is less barrier faced by the carriers for this reason threshold voltage decreases as shown in figure.

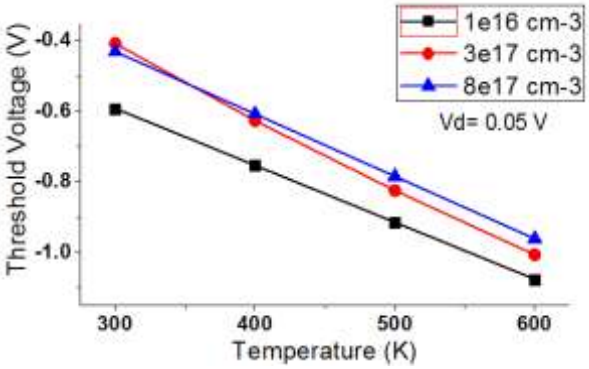

Figure 4. Threshold variation with temperature range from 300 to 600 K.

Figure 5 shows that transconductance decreases with increasing the temperature, The reason is that due to the phonon scattering and columbic scattering there is a fall in mobility so the drain current decrease. When the temperature becomes lower, then the transconductance turns into higher value [10]. This is because of the less mobility degradation due to the minimum collisions. At higher channel doping concentration there is maximum scattering whereas at lower doping concentration scattering is minimum. That's why at lower doping concentration drain current becomes higher which enhances the transconductance clearly shown in figure 5.

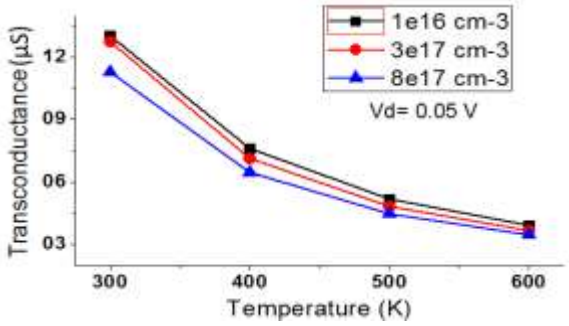

Figure 5. Dependence of transconductance on temperature at 0.05 V of drain voltage.

The degradation of the current with the enhancement of the temperature is due to the increase in collision between carriers and lattice. At higher temperature there is maximum mobility degradation. So, the drain current becomes low. Figure 6 shows that how current decreases with the rise of the temperature. At high drain voltage, the drain current is high because of the generated electron-hole pairs produced by the impact ionization [11]. These newly generated electrons collide with the more lattice atoms to produce more electron-hole pairs. This generation process repeats itself. As a result, the drain current quickly amplified as shown in figure 6.

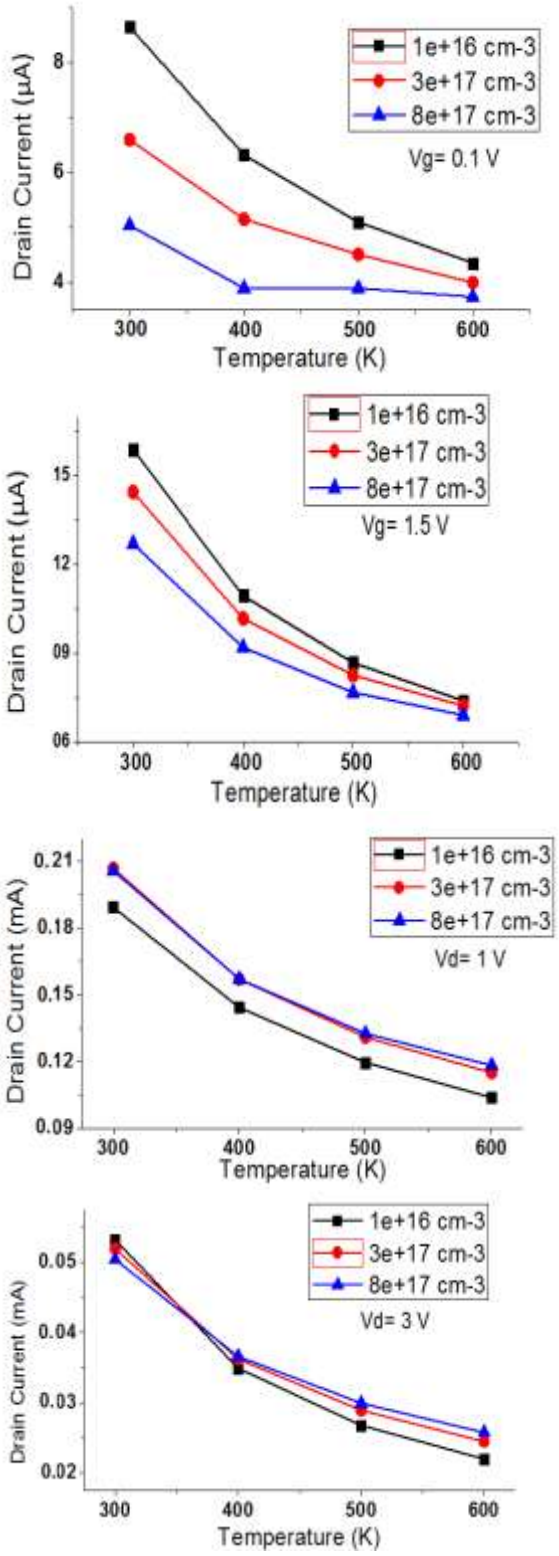

Figure 6. Variations of drain current with respect to temperature at different gate and drain voltages.

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IV. CONCLUSIONS

The effect of temperature on the impact ionization of the n-channel FD SOI MOSFET has analyzed. By the simulation results, we have observed that impact ionization decreases with the increase of the temperature. Furthermore, threshold voltage and transconductance has also studied at different temperature with fixed channel doping concentration .We have found that threshold voltage and the transconductance are inversely proportional to the temperature. This simulation suggests that n-channel FD SOI MOSFET has a considerable advantages for high temperature.

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